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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/564,079	01/09/2006	Ernst Bretschneider	DE03 0241 US1	7528

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EXAMINER	
PARIHAR, SUCHIN	
ART UNIT	PAPER NUMBER
2825	

NOTIFICATION DATE	DELIVERY MODE
07/01/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/564,079	BRETSCHNEIDER, ERNST	
	Examiner	Art Unit	
	SUCHIN PARIHAR	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/9/2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/9/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. **Claim 14 is rejected under 35 U.S.C. 112, second paragraph**, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. With respect to claim 14, the "optical tracing" limitation recited in claim 14 is considered a descriptive attribute or characteristic of the optical tracing itself, however no "optical tracing" step is recited in the parent claim(s). Additionally, the phrase "the optical tracing" lacks antecedent basis in the claims.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 1-13 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Lippmann et al. (2003/0127709) in view of Baukus et al. (6,613,661).

6. With respect to claim 1, Lippmann teaches:

a security-sensitive (security critical ICs, paragraph [0006]) semiconductor product, particularly a smart-card chip (smartcard, paragraph [0006]), in which not only are produced electrically active structures (active devices, paragraph [0002])

envisaged by the chip design (internal structure of the semiconductor chip, paragraph [0004]) in the form of circuit functions (important functions of the chip, paragraph [0030]) in and on a wafer (each chip on the wafer, paragraph [0099]), which may for example be composed of silicon (polysilicon, paragraph [0040]), but also additional, electrically conductive parts (electrically conductive polymer, paragraph [0012]), which are insulated from one another (insulator covering, paragraph [0029]), are generated as a filling structure (filling the clearance with material, see Lippmann, claim 35), characterized in that the parts of the filling structures that are generated are combined with contacts (contacts that are separated and isolated from one another, paragraph [0002]).

Lippmann fails to explicitly teach:

additional circuit functions are generated as well as the circuit structures that are produced for the circuit.

However, Baukus teaches: additional circuit functions are generated (additional circuit elements that do not contribute toward the desired circuit function are added to an IC, Col 1, lines 25-40) as well as the circuit structures that are produced for the circuit.

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Baukus into the invention of Lippmann for at least the following reason: Baukus improves the security enhancement of Lippman (security-critical IC's, see Lippmann, paragraph [0006]) by providing a technique to further frustrate attempts to reverse engineer an IC such as to add additional circuits such as dummy circuitry to

prevent reverse engineering which is a desirable achievement in the art (see Baukus, Col 1, lines 1-40).

7. With respect to claim 2, Lippmann teaches:

characterized in that the parts of the filling structures (filling the clearance with material, see Lippmann, claim 35) that are generated are composed of metal, of polycrystalline silicon (polysilicon, paragraph [0040]), of diffusion regions, or of other electrically conductive materials of the semiconductor product (semiconductor device, paragraph [0002]).

8. With respect to claim 3, Lippmann teaches:

characterized in that the contacts are also set by a routing program belonging to a design program for chip design (provided for the wiring, paragraph [0036]).

9. With respect to claim 4, Lippmann teaches:

characterized in that the passive fill structures composed of metal are connected together electrically, so that at least one closed signal path is formed between two or more nodes of the active circuitry of the circuit (plated-through paths to be established by vertical electrically conducting connections, paragraph [0066]).

10. With respect to claim 5, Lippmann teaches:

characterized in that the contacts are set in such a way that arbitrary interlinkings, both horizontal and vertical, of the parts of the fill structure are produced (see Lippmann, figures 6 and 7).

11. With respect to claim 6, Lippmann teaches:

characterized in that the contacts are set in such a way that after each part of the fill structure the wiring level is changed and the horizontal direction is changed within the level (contacts that are separated and isolated from one another by intermetal dielectrics, paragraph [0002]).

12. With respect to claim 7, Lippmann teaches:

characterized in that substantially the major proportion of the fill structures generated are incorporated in the signal path, so that active, electrically connected parts of the fill structures are even situated next to dummy fill structures that are insulated from the active electrically connected parts of the fill structures (see Lippmann, figures 6 and 7).

13. With respect to claim 8, Lippmann teaches:

characterized in that the signal path is connected to further suitable integrated electronic circuit components such as, for example, transistors, diodes, resistors and capacitors (multi-layered resistance network, paragraph [0009]; transistor function, see Abstract).

14. With respect to claim 9, Lippmann teaches:

characterized in that the signal path that is composed of parts of the fill structures that are interlinked with one another is used as a supply track by connecting electronic circuit components, such as transistors, diodes, resistors, capacitors or opto-electrical components, to the supply voltage via the parts of the fill structures that are interlinked with one another (multi-layered resistance network, paragraph [0009]; transistor function, see Abstract).

15. With respect to claim 10, Baukus teaches:

characterized in that the signal path that is composed of parts of the fill structures that are interlinked with one another is used as a supply-to-ground path by causing the parts of the fill structures that are interlinked with one another to form an electrically conductive current path between the supply voltage and the ground potential of the electronic circuitry (see Figures 1a and 1b).

16. With respect to claim 11, Lippmann teaches:

characterized in that a pick-off, which may be fed to electronic analyzer circuits, takes place between two contacts at a time on the signal path (contacts pick off a Hall voltage, paragraph [0017]).

17. With respect to claim 12, Lippmann teaches:

characterized in that the signal path that is composed of parts of the fill structures that are interlinked with one another is used as a resistive signal path, in which case the parts of the fill structures that are interlinked with one another are connected between the supply voltage and the ground potential of the electronic circuitry and, as well as this, semiconductor resistors are inserted in this path at random intervals by means of contacts that are set (multi-layered resistance network, paragraph [0009]; transistor function, see Abstract).

18. With respect to claim 13, Lippmann teaches:

characterized in that a pick-off, which may be fed to electronic analyzer circuits, takes place between two resistors at a time (contacts pick off a Hall voltage, paragraph [0017]).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SUCHIN PARIHAR whose telephone number is (571)272-6210. The examiner can normally be reached on Mon-Fri, 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jack Chiang/
Supervisory Patent Examiner, Art Unit 2825

/Suchin Parihar/
Examiner, Art Unit 2825